Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method comprising:

determining whether a register of a processor has been updated; and

if the register is updated, setting an indicator bit.

Claim 2 (currently amended): The method of claim 1 including determining whether the register has been updated by checking [[an]] the indicator bit.

Claim 3 (original): The method of claim 2 wherein if the register has not been updated, refraining from transferring the contents of the register back to a memory.

Claim 4 (original): The method of claim 2 including determining whether the register has been updated and if so, saving the contents of the register to memory.

Claim 5 (original): The method of claim 4 including saving the register contents to memory on a context change.

Claim 6 (currently amended): The method of claim 1 including assigning a single indicator bit as the indicator bit for [[to]] a plurality of registers.

Claim 7 (currently amended): An article comprising a medium storing machine-readable instructions that if executed enable a processor-based system to:

determine whether a register of a processor of the processor-based system has been updated; and

if the register is updated, set an indicator bit.

Claim 8 (currently amended): The article of claim 7 further storing instructions that enable the processor-based system to determine whether the register has been updated by checking [[an]] the indicator bit.

Claim 9 (original): The article of claim 8 further storing instructions that enable the processor-based system to refrain from transferring the contents of the register back to a memory if the register has not been updated.

Claim 10 (original): The article of claim 8 further storing instructions that enable the processor-based system to determine whether the register has been updated and if so, save the contents of the register to memory.

Claim 11 (original): The article of claim 10 further storing instructions that enable the processor-based system to save the register contents to memory on a context change.

Claim 12 (currently amended): The article of claim 10 further storing instructions that enable the processor-based system to save the contents of a plurality of registers to memory if [[an]] the indicator bit is set.

Claim 13 (currently amended): A processor comprising:

a register; and

a storage storing instructions to determine whether [[a]] the register has been updated and if the register is updated, set an indicator bit.

Claim 14 (currently amended): The processor of claim 13 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking [[an]] the indicator bit.

Claim 15 (original): The processor of claim 14 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to a memory.

Claim 16 (original): The processor of claim 14 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to memory.

Claim 17 (original): The processor of claim 16 wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change.

Claim 18 (currently amended): The processor of claim 13 including a second storage to store said indicator bit.

Claim 19 (currently amended): A system comprising:

~~a processor;~~

a processor having a register ~~coupled to said processor~~; and

a storage to store ~~storing~~ instructions to determine whether [[a]] the register has been updated and if the register [[is]] has been updated, set an indicator bit.

Claim 20 (original): The system of claim 19 including a memory and an interface between said memory and said processor.

Claim 21 (currently amended): The system of claim 20 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking [[an]] the indicator bit.

Claim 22 (original): The system of claim 21 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to the memory.

Claim 23 (original): The system of claim 21 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to the memory.

Claim 24 (original): The system of claim 23 wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change.

Claim 25 (currently amended): The system of claim 19 including a second storage to store said indicator bit.

Claim 26 (currently amended): The system of claim 19 including a control register to store said indicator ~~storing said~~ bit and wherein said storage storing instructions and said control register are part of said processor.

Claim 27 (currently amended): The system of claim 19 including a plurality of registers coupled to said processor and a single indicator bit as the indicator bit for all of those registers.

Claim 28 (new): The method of claim 5, further comprising not saving the register contents to memory on the context change if the register has not been updated.

Claim 29 (new): The article of claim 11, further comprising instructions that enable the processor-based system to not save the register contents to memory on the context change if the register has not been updated.

Claim 30 (new): The processor of claim 18, wherein said register includes said second storage.

Claim 31 (new): The processor of claim 30, wherein said register comprises a control register.

Claim 32 (new): The system of claim 25, wherein said register includes said second storage.

Claim 33 (new): The system of claim 32, wherein said register comprises a control register.